



TSMC Reduces Chip Defects

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The semiconductor maker has developed ways to minimize problems in a new manufacturing method.
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Taiwan Semiconductor Manufacturing said Wednesday it's developed techniques to reduce chip defects when it tested a new chip-making process that is expected to be widely used by the semiconductor industry in the next few years.

TSMC, the world's largest contract chip maker, said its researchers have found ways to minimize problems caused by immersion lithography, a manufacturing technology that employs water in the process of using light to imprint circuits on a silicon wafer.

After circuits are printed on the wafer, the wafer is cut into pieces to create the chips that you find inside electronic devices.

"With defect root causes understood, TSMC can now focus on throughput improvement for high-volume manufacturing," said Burn Lin, senior director of TSMC's micropatterning division. The company plans to discuss its findings at the SPIE Microlithography Conference in San Jose, California, on Thursday.

Until now, tools have been available to produce chips without using water. But putting even finer circuitry on a wafer will require new equipment.

For years, equipment makers have been developing replacement tools called extreme ultraviolet lithography (EUVL). But those tools are expensive and still unproven, and they represent a dramatic departure from the current manufacturing technology.

Instead of using EUVL, researchers have found ways to improve on the current method, using water as an aide. The water enables lithography equipment to beam light with a shorter wavelength, which is more focused and able to print smaller circuitry. This immersion lithography gives the industry several more years to improve the EUVL technology.

But immersion lithography has its own problems: water bubbles or particles that appear during the circuitry-printing process can cause wafer defects and unusable chips. TSMC researchers have been able to develop techniques to reduce the defects down to three per wafer.

"TSMC has done extraordinarily well" in cutting down on defects, said Dave Cavanaugh, an analyst with Semico Research. "They have control of their process."

Being able to control defects will allow TSMC to use immersion lithography in mass-producing chips at 45 nanometer, which refers to the average size of the features on a chip. Each nanometer is a billionth of a meter. TSMC hasn't said when it will start the 45 nm process.

Costly Gear

Equipment for immersion lithography isn't cheap. Each unit costs between \$20 million and \$25 million, Mr. Cavanaugh said.

ASML, a Netherlands-based equipment maker, on Wednesday said it plans to start producing a new generation of immersion lithography equipment in the second quarter. Its previous generations of equipment have been used mostly in labs by companies such as TSMC that want to test the tools.

Some chip companies with their own manufacturing facilities also plan to use immersion lithography. On Monday, IBM researchers said they, too, have discovered ways to make immersion lithography work.

On the other hand, Intel, the world's largest chip maker, said it doesn't plan to use immersion lithography for 45 nm but will consider it for 32 nm. Currently Intel is using 65 nm to produce its computer processors.

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