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Samsung Slims Memory Chip Stack

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Previous stacking approaches have been hampered by the need to put interconnect wiring along the sides of the stack. Samsung, however, is using laser-cut, micron-sized holes to connect the circuits, eliminating the need for gaps and the protruding wiring, the company said.

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South Korean electronics and semiconductor giant Samsung claimed a three-dimensional, stacked memory chip breakthrough this week with new technology that shrinks the space needed for stacked chip layers used in mobile phones and other devices.

Samsung said by stacking eight 2 gigabit NAND flash memory chips, it could deliver a smaller-footprint wafer-level processed stack package (WSP), a method of stacking silicon chip dies to increase performance while economizing space and energy requirements.

Although the stack approach is fairly common and includes mixed stacks of different types of memory or other chips, Samsung has indeed made a breakthrough by putting holes in the stacked dies for more efficient interconnections, Semico Vice President of Strategic Technologies Morry Marshall told TechNewsWorld.

"It has tremendous potential for cell phones because space is so limited," Marshall said. "I expect Samsung will have tremendous penetration with this."

Process Breakthrough

Previous stacking approaches have been hampered by the need to put interconnect wiring along the sides of the stack. Samsung, however, is using laser-cut, micron-sized holes to connect the circuits, eliminating the need for gaps and the protruding wiring, the company said.

Intel (Nasdaq: INTC) reportedly referenced the approach, known as "through silicon via," at its developer forum last year, but Samsung is the first to succeed in stacking and connecting with holes, according to Marshall.

"The real breakthrough they've made here is the reliable through-hole via," he said. "I'm not aware of any other successful through-holes. That's the breakthrough really."

Smarter Stack

Other chip makers have typically sought to stack chip dies to keep bumping up performance without taking more space, which is becoming more and more critical for sophisticated cell phones, smartphones, and other mobile devices.

Chip makers have also combined RAM, flash, and other memories with stacks, but have historically been restrained by the added space requirements of wiring that connects the layers.

"This technology has the potential to replace all of those different kinds of stacking things because it has a smaller footprint," Marshall said.

The analyst added while Samsung typically keeps its silicon and cell phone businesses separate, it is a leading mobile phone maker, and will likely find a receptive market for the space-saving technology.

Moore's Law

Although silicon processors have largely been able to maintain Moore's Law of doubled data density every 18 months by shrinking components and building out, there is sometimes a need to build up, Gartner Research Vice President Martin Reynolds told TechNewsWorld.

"It's an obvious extension if you can go up instead of out," he said. "The thing is, 'out' for the most part has been doing the job."

Reynolds agreed the big challenge of chip stacks is the interconnect wiring, and said eventually, all semiconductor technology may take on a three-dimensional look.

"I could see one day everything going vertical, but not for some time," he said.

The Look of Things Now

The new Samsung technology, which will initially be used for NAND-based memory cards early next year, also allows the use of identical chips oriented in the same way, as opposed to being staggered or separated to allow for wiring, Semico analyst Jim Handy told TechNewsWorld.

The stack approach continues to hold more value as the demand for performance and functionality goes up with expectations of even smaller devices, he said.

"It's certainly becoming the way things are done nowadays," he said.

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