

Challenges at 28nm and Below For First-Time Silicon Success

Analog Bits believes there are two components to the 28nm Challenge: Technical Challenges and Business Challenges. Mahesh Tirupattur will chair the panel that will consist of a 28nm design customer, a foundry representative, an EDA tool partner and a high-end IP company. Panel members will include five parties including:

Moderator: Mahesh Tirupattur

*Executive Vice President
Analog Bits*

Chi-Ping Hsu, Ph.D.

*Senior Vice President, Research and Development, Silicon Realization Group
Cadence*

Mark Papermaster

*Vice President, Switching Silicon Technology Group
Cisco*

Grant Pierce

*President & CEO
Sonics*

Speaker TBA
TSMC

The panel will explore aspects of the challenge of designing and manufacturing leading edge ICs. The semiconductor market is a fast-moving competitive environment that is increasingly communication and consumer driven with a strong drive to provide increasing performance and bandwidth in a reduced power environment. Analog Bits will moderate this panel. The panel will discuss the critical issues in coordinating EDA challenges with customer design requirements, challenges in efficiently connecting multi IP blocks and resulting in a manufacturable high yielding IC on time and on budget to hit the market window.

